REMARKS

STATUS OF THE CLAIMS

In accordance with the foregoing, claims 2, 3, 5, 11-13 and 15-17 have been amended. Claims 1-20 are pending and under consideration.

No new matter is being presented, and approval of the amended claims is respectfully requested.

REJECTIONS OF CLAIMS 1-20 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) AS BEING UNPATENTABLE OVER FARRELL (U.S. PATENT NO. 5,014,195) AND COLLINS (U.S. PATENT NO. 5,848,428) IN VIEW OF ALBONESI (DAVID H. ALBONESI, "SELECTIVE CACHE WAYS: ON-DEMAND CACHE RESOURCE ALLOCATION," 1999)

The rejections of claims 1-20 are respectfully traversed and reconsideration is requested.

On page 4 of the Action, the Examiner notes that Farrell does not teach the newly-added feature of consumption power mode control units in number n, individually controlling each cache memory section, as recited in independent claims 1, 5, 11 and 15. However, the Examiner cites Collins as disclosing this feature.

Applicants respectfully disagree with the Examiner's understanding of the disclosure of Collins. Collins discusses a multiple-way cache memory system that selectively enables sense amplifiers in a given memory bank when the memory bank contains data that is being accessed. (Abstract). Each memory bank (300, 302, 304 and 306) has one or more sense amplifiers 352, which are a source of power consumption in the cache memory system. In order to enable a particular bank of sense amplifiers 352, each bank receives one of the sense amplifier control signals generated by the sense amplifier control circuit 320. (See column 10, lines 33-43, and Figs. 3 and 4).

Therefore, in Collins, only <u>one</u> sense amplifier control circuit 320 controls all the sense amplifiers with a respective sense amplifier control signal. Thus, Collins does not teach or even suggest consumption power mode control units in number n, individually controlling each cache memory section, as recited in independent claims 1, 5, 11 and 15.

Since each cache memory section, according to the present invention, has an individual consumption power mode control unit (i.e., consumption power mode control devices 40a, 40b, 40c, 40d, 41a, 41b, 41c and 41d), which are arranged in the cache memory system (as opposed to the power control unit), the entire power consumption can be reduced by limiting the number of cache memories that are turned on (and, therefore, consuming electric power). (See Fig. 4, page 22, lines 11-22 and page 24, line 21 to page 25, line 7 of the Specification).

Furthermore, the cache memories can be turned on or off simultaneously (and, therefore, quickly) because each of the consumption power mode control units controls each of the cache memories in parallel. Moreover, operational delay can be reduced because each of the consumption power mode control units can be arranged near its respective cache memory section. (See Fig. 4).

Therefore, it is respectfully submitted that independent claims 1, 5, 11 and 15, as well as the pending dependent claims, patentably distinguish over the prior art.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. Further, all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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